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EXAMINER	
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ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/620,515	VARTTI ET AL.	
	Examiner	Art Unit	
	Lev I. Iwashko	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendments made Claims 1, 12, 22, and 30 have been acknowledged.

2. Claims 1-32 stand rejected.

Claim Rejections - 35 USC § 102

3. The following are quotations of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 12-20, and 22-32 are rejected under U.S.C. 102(b) as being anticipated by Baror (US Patent 5,627,992)

Claim 12. A memory system, comprising:

- first memory logic; *(Figure 3, number 305 – Shows Memory Address Logic)*
- at least one other memory; *(Figure 1, numbers 102 and 190 – Show a data cache and a memory respectively)*
- a storage device coupled to the first memory logic to store a programmable indicator identifying a mode of referencing the first memory logic and the at least one other memory; and *(Column 50, lines 36-67 – State that there is a control unit (which store the memory logic) coupled to the block status array (which is a plurality of storage locations), and the control unit is configured to store "a value indicative of a write-through write mode into said status field of a particular one of a plurality of storage locations)*
- a control circuit coupled to the first memory logic and the at least one other memory, the control circuit to receive a request for data, copies

of which may be resident within the first memory logic and the at least one other memory, and in response thereto, to determine based on the identified mode whether to attempt to retrieve the requested data from of the first memory logic, the at least one other memory, or both the first memory logic and the at least one other memory. *(Column 51, lines 57-67 and Column 52, lines 1-12 – State that there is a control circuit performs a write-through operation is response to a write hit to a particular cache block associated with a cache-block status field which indicates said copy-back state)*

Claim 13. The system of Claim 12, wherein the first memory logic includes at least one of a tag memory and a memory to store data. *(Column 5, lines 61-67)*

Claim 14. The system of Claim 12, wherein the control circuit includes a circuit to determine whether the programmable indicator is in a first predetermined state, and if so, to further determine whether the at last one other memory must be referenced to complete the request, and if not, to obtain the data from the first memory logic without reference to the at least one other memory. *(Column 51, lines 57-67 and Column 52, lines 1-18- State that there is a control circuit that is "configured to set said state of said cache block status flied to indicate said write-through write mode if said first input line conveys said write-through status, even if said TLB write policy field is set in said second TLB write policy field)*

Claim 15. The system of Claim 14, wherein the control circuit includes a circuit to initiate references to both the first memory logic and the at least one other memory if the at least one other memory must be referenced to complete the request. *(Column 54, lines 18-27 – State that the control circuit is configured to perform a write-through operation associated with a cache block status field, ands stores data in a particular cache data subsystem)*

Claim 16. The system of Claim 12, wherein the control circuit includes a circuit to determine whether the programmable indicator is in a second predetermined state, and if so, to initiate a reference to the first memory

logic and the at least one other memory irrespective of whether a reference to the at least one other memory is necessary to complete the request. *(Column 52, lines 59-64 – State that if the TLB write policy field is in the second state, then the policy-pins are placed into the first state regardless)*

Claim 17. The system of Claim 12, wherein the control circuit includes a circuit to determine if the programmable indicator is in a third predetermined state indicating the first memory logic is unavailable for storing data, and if so, to initiate a reference to the at least one other memory without attempting to obtain the requested data from the first memory logic. *(Column 13, lines 7-13 – State that there is a third state that indicated the program mode during memory access. Also, the "ICU transfers the value presented on the processor bus to the memory bus")*

Claim 18. The system of Claim 12, wherein the first memory logic includes a shared cache, wherein the at least one other memory includes one or more dedicated caches, and further comprising at least one instruction processor coupled to the one or more dedicated caches. *(Column 7, lines 11-20)*

Claim 19. The system of Claim 12, and further comprising a main memory coupled to the first memory logic to issue the request for the data. *(Column 45, lines 40-42 – State that there is logic that should be capable of monitoring all main memory accesses)*

Claim 20. The memory system of Claim 12, and further including mode switch logic coupled to the storage device to automatically re-program the programmable indicator. *(Column 25, lines 24-37 – State that there is a method to switch between two caches for programming)*

Claim 22. A method for use in a data processing system having a first memory coupled to at least one other memory and a programmable storage device, the programmable storage device to identify a reference mode to control the manner in which data is retrieved from at least one of the first memory and the at least one other memory, the method comprising: *(Column 50, lines 36-67 – State that there is a control unit (which store the memory*

logic) coupled to the block status array (which is a plurality of storage locations), and the control unit is configured to store "a value indicative of a write-through write mode into said status field of a particular one of a plurality of storage locations)

a.) receiving a request for data, copies of which may be stored within at least one of the first memory and the at least one other memory; and *(Column 8, line 62 – Discloses a data request. Column 50, lines 44-45 – State that there is a first input configured to convey a first write-through status value)*

b.) based on the reference mode, initiating an operation to attempt to retrieve the requested data from the first memory, the at least one other memory, or from both the first memory and the at least one other memory.

Claim 23. The method of Claim 22, wherein step b.) comprises:

- if the reference mode selects a first mode, determining whether the request can be completed without accessing the at least one other memory; *(Column 2, lines 42-44 – State that the cache block status field indicate whether or not the cache is shared or exclusive, thereby signifying whether or not other memories must be accessed)*
- and if the request can be completed without accessing the at least one other memory, obtaining the requested data from the first memory. (Column 2, lines 44-47 – State that the cache block status field controls which mode the control unit operates in)

Claim 24. The method of Claim 22, wherein step b.) comprises:

- if the reference Mode selects a first mode, determining whether the request can be completed without accessing the at least one other memory; *(Column 2, lines 42-44 – State that the cache block status field indicate whether or not the cache is shared or exclusive, thereby signifying whether or not other memories must be accessed)*

- and if the request cannot be completed without accessing the at least one other memory, initiating references to the first memory and the at least one other memory to complete the request.

Claim 25. The method of Claim 22, wherein if the reference mode selects a second mode, initiating a reference to the first memory and the at least one other memory irrespective of which of the first memory or the at least one other memory stores the data. *(Column 31, lines 22-30 – State that a first word is written into the cache during the second cycle and deals with the buffer)*

Claim 26. The method of Claim 22, wherein step b.) comprises:

- determining that the first memory is unavailable to store the requested data; *(Column 34, lines 42-44 – State that the requested data cannot be stored in the cache array)*
- and obtaining the requested data from the at least one other memory. *(Column 34, lines 32-39 – State that a variable or instruction may be fetched from a four word read buffer)*

Claim 27. The method of Claim 22, and further including modifying the reference mode based on conditions within the data processing system. *(Column 4, lines 64-67 – State that there is a "block modified relative to the main memory")*

Claim 28. The method of Claim 22, wherein the data processing system includes a main memory coupled to the first memory, *(Column 53, lines 44-45 – State that there is write buffer coupled to the storage array)*

- and wherein step a.) includes receiving a request for data from the main memory. *(Column 8, line 62 – Declares a data request)*

Claim 29. The method of Claim 22, wherein the at least one other memory includes multiple coupled memories, and wherein step b.) comprises *(Column 53, lines 44-45 – State that there is write buffer coupled to the storage array)*

- issuing a request for the requested data to the multiple coupled memories; *(Column 12, lines 33-34 – State that the ICU uses the signals as outputs)*

- and receiving the requested data from one of the multiple coupled memories. *(Column 12, lines 34-36 – State that the ICU uses the signals as inputs)*

Claim 30. A data processing system, comprising: *(Column 3, lines 35 – Discloses a RISC processing system)*

- main memory means for storing data; *(Column 3, lines 62-63 – A main memory is disclosed)*
- first cache means for storing a first sub-set of the data; second cache means for storing a second sub-set of the data; *(Column 3, line 40 – States that there are two ICUs (integrated cache units))*
- programmable storage means for storing one or more control signals to control the way in which data is retrieved from the first cache means and the second cache means; and *(Column 7, lines 59-64)*
- control means for receiving requests from the main memory means requesting return of data, the control means further for initiating a reference to retrieve that data from one or both of the first and second cache means based, at least in part, on the state of the one or more control signals. *(Column 51, lines 57-67 and Column 52, lines 1-12 – State that there is a control circuit performs a write-through operation is response to a write hit to a particular cache block associated with a cache-block status field which indicates said copy-back state)*

Claim 31. The system of Claim 30, and further including mode switch means for monitoring system conditions and automatically altering one or more of the control signals based on the system conditions. *(Column 25, lines 15-23 – State that the instruction can be "issued as part of the context switch procedure", which means that the cache configuration is reconfigured utilizing an easy method)*

Claim 32. The system of Claim 30, wherein the first cache means includes tag means for storing tag information describing the first sub-set of the data; *(Column 5, lines 61-65)*

- and wherein the control means includes means for initiating a reference to one or both of the first and 4 the second cache means based, at least in part, on tag information for the requested data. *(Column 5, lines 62-64 – State that "a cache tag is associated with each block, and it is stored in the cache array")*

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 1 is rejected under 35 U.S.C.103(a) as being unpatentable over Luan et al. further in view of Chapin et al. (US Patent 6,496277).

Luan teaches a portion of the limitations of claim 1 as follows:

A memory System, comprising: *(Abstract, line 2 – Discloses a memory system)*

- a first storage device; *(Figure 1A, number 104 – Shows a storage device)*
- at least one additional storage device; *(Figure 1A, number 107 – Shows an additional storage device)*
- a control storage device to store a programmable indicator identifying the manner in which the first and the at least one additional storage device are to be referenced; and *(Column 4, lines 44-48 – Disclose a system controller which is coupled to each memory configuration controller (control storage device))*
- a control circuit coupled to the first storage device, the at least one additional storage device, and the control storage device, *(Column 4, lines 49-54 – State that there is a memory configuration controller that*

is coupled to the shared memory, associated memory, and system controller)

- the control circuit to receive a request for data, *(Column 4, lines 52-54 – Disclose a signal received to the memory configuration controller)*
- and in response to the request, to attempt to retrieve the requested data by initiating, based on the state of the programmable indicator, at least one of a first reference to the first storage device and a second reference to the at least one additional storage device. *(Column 4, lines 56-60)*

Luan's invention differs from the claimed invention in that there is no specific reference to copied data.

Luan fails to teach the portion of claim 1 which states "wherein copies of the requested data may be stored within the first and the at least one additional storage device." However, Chapin's invention discloses the following: "As indicated at 136, the system controller 46 also responds to the presence of a user interface request from the touch screen display 56, the keyboard 58 and the mouse 60 of the user interface 44. If there is a request, the system controller 46 retrieves a copy of the image data from the system memory 20 and transfers that copy to the user interface 44 for display (steps 138 and 140). If there are no requests, the facility 15 then determines if there are any print requests" (Column 13, lines 50-58). It would have been obvious to one of ordinary skill in the art, having the teachings of the "Shared Memory Apparatus" of Luan and Chapin's "Data Flow Control and Storage Facility" before him at the time the invention was made, to combine the two inventions to allow for copied data to be stored in two storage devices so that there would be a backup data preservation mechanism.

7. Claims 3-4 and 6-10 are rejected under 35 U.S.C.103(a) as being unpatentable over Luan et al. as applies to Claim 1 above, further in view of Chapin et al. (US Patent 6,496277).

Luan teaches Claim 1 as stated above.

The following is a listing of the Claims and how they are rejected by Luan:

Claim 3. The system of Claim 1, wherein if the programmable indicator is in a first state, the second reference is issued only if the first reference is not capable of completing the request. *(Column 4, lines 59-60 – Disclose that the memory configuration controller couples the memory I/O port to the HPB, pending that the there is no coupling to the SMB)*

Claim 4. The system of Claim 3, wherein if the programmable indicator is in a second state, the second reference is issued regardless of whether the second reference is required to complete the request. *(Column 5, Table 2 – Shows that whether or not the "Select" is a "1" or a "0", the "OE" will be "1")*

Claim 6. The system of Claim 1, and further including mode switch logic to modify the state of the programmable indicator between the first state and the second state based on programmable criteria. *(Column 4, lines 56-67 – Disclose a mode select control signal and memory configuration controllers which modify the states)*

Claim 7. The system of Claim 6, wherein the control circuit receives multiple requests for data, (*Column 11, line 1 – States that there are configuration requests)*

- and wherein the mode switch logic includes a circuit to modify the state of the programmable indicator from the first state to the second state if at least a first predetermined number of the multiple requests requires the second reference to complete. *(Column 2, lines 33-45 – State that the programmable shared memory dynamically configures the memory during start up during a memory configuration request. In other words, the states are changed)*

Claim 8. The system of Claim 7, wherein the mode switch logic includes a circuit to

modify the state of the programmable indicator from the second state to the first state if a second predetermined number of the multiple requests does not require the second reference to complete. *(Column 2, lines 33-45 – State that the programmable shared memory dynamically configures the memory during start up during a memory configuration request. In other words, the states are changed)*

Claim 9. The system of Claim 8, wherein the mode switch logic includes a circuit that allows at least one of the first and the second predetermined numbers to be programmably selected. *(Column 2, line 42 – States that this is programmable architecture)*

Claim 10. The system of Claim 8, and further including a main memory coupled to the first storage device to issue the request to the control circuit. *(Column 9, lines 1-3 – State that the associated memory is coupled to the processor bus)*

8. Claims 2 and 5 are rejected under 35 U.S.C.103(a) as being unpatentable over Luan et al. as applied to claims 1 and 3-4 above.

Luan teaches the limitations of claims 1 and 3-4 for the reasons above.

Luan's invention differs from the claimed invention in that there is no specific reference to the order in which the references are issued in regards to the states.

Luan fails to teach claims 2 and 5, which respectively state "The system of Claim 1, wherein the first and the second references are issued in a time order that is controlled by the state of the programmable indicator", and "The system of Claim 4, wherein if the programmable indicator is in the second state, the second reference is issued before the first reference." However, stating that there is a sequence in which things must occur does not change the purpose or functionality of the claimed invention. Therefore, it would have been obvious to one

of ordinary skill in the art to enable Luan's "Shared Memory" to have the indicator controlled by a time order and by changing state orders.

For further information, reference Ex parte Rubin , 128 USPQ 440 (Bd. App. 1959) (Prior art reference disclosing a process of making a laminated sheet wherein a base sheet is first coated with a metallic film and thereafter impregnated with a thermosetting material was held to render prima facie obvious claims directed to a process of making a laminated sheet by reversing the order of the prior art process steps.). See also In re Burhans, 154 F.2d 690, 69 USPQ 330 (CCPA 1946) (selection of any order of performing process steps is prima facie obvious in the absence of new or unexpected results); In re Gibson, 39 F.2d 975, 5 USPQ 230 (CCPA 1930) (Selection of any order of mixing ingredients is prima facie obvious.).

9. Claim 11 is rejected under 35 U.S.C.103(a) as being unpatentable over Luan et al. as applied to claims 1, 6-8, and 10 above, further in view of Baror. (US Patent 5,627,992).

Luan teaches the limitations of claims 1, 6-8, and 10 or the reasons above.

Luan's invention differs from the claimed invention in that there is no specific reference to a memory map.

Luan fails to teach claim 11, which states "The system of Claim 10, wherein the request is requesting data associated with one or more incomplete memory coherency actions, and further comprising a request tracking circuit coupled to the control circuit to track the incomplete memory coherency actions, whereby the data is returned to the main memory only after all of the coherency actions are completed." However, Baror's invention discloses the following: "Ownership--This is a scheme to guarantee data consistency. The most current value of a variable is owned by one cache or the main memory. It is the responsibility of the owner to

maintain the consistency of the variable. There are several ownership schemes which differ in the number of states that are attributed to a variable and the algorithms for ownership and state transitions." (Column 7, lines 6-11). It would have been obvious to one of ordinary skill in the art, having the teachings of the "Shared Memory Apparatus" of Luan and Baror's "Integrated Cache Unit" before him at the time the invention was made, to allow cache coherency to occur by utilizing a tracking device, since cache coherency is vital for a system to run efficiently and without error.

10. Claims 21 is rejected under 35 U.S.C.103(a) as being unpatentable over Baror (US Patent 5,627,992) as applied to claims 12 and 20 above.

Baror teaches the limitations of claims 12 and 20 for the reasons above.

Baror's invention differs from the claimed invention in that there is no specific reference to the automating of the programming process.

Baror fails to teach claim 21, which states "The memory system of Claim 20, wherein the mode switch logic includes a circuit to monitor conditions within the memory system, and to automatically re-program the programmable indicator based on the monitored conditions." However, Baror does state that "The Chip Select Mapping Register...specifies the address and the conditions for the ICU chip and its functions" (Column 17, lines 21-25)." Therefore, stating that the above is done automatically does not change the purpose or functionality of the claimed invention. Therefore, it would have been obvious to one of ordinary skill in the art to enable Baror's "Integrated Cache Unit" to automate the re-programming in order to make the whole programming process faster and more user-friendly.

For further information, reference Venner, 262 F.2d 91, 95, 120 USPQ 193, 194 (CCPA 1958) (Appellant argued that claims to a permanent mold casting apparatus for molding trunk pistons were allowable over the prior art because the claimed invention combined "old permanent-mold structures together with a timer and solenoid which automatically actuates the known pressure valve system to release the inner core after a predetermined time has elapsed." The court held that broadly providing an automatic or mechanical means to replace a manual activity which accomplished the same result is not sufficient to distinguish over the prior art.).

Response to Arguments

11. Applicant's arguments (filed February 16, 2006) with respect to claims 1-32 have been considered but are moot in view of the previous, new and following ground(s) of rejection.

12. With regards to Claim 1, the Applicant alleges that the "Luan control circuit is coupled to exactly one memory 104, and not to any additional memory". However, Luan clearly shows in both Figure 1A and Figure 2, a Component 106 known as the "Peripheral Controller". This "Peripheral Controller" is shown to be coupled to the "Dedicated Peripheral Memory" (Figure 1A, Component 107), as well as the "Memory Configuration Controller" (Figure 2, component 202). Therefore, Figures 2 and 1A clearly show how the components are successfully coupled together. Finally, if the Applicant has further reason not to honor the above argument, the Examiner respectfully presents Figure 4, Components 412, 202 and 104. This Figure clearly shows two separate memories (412 and 104) coupled to the "Memory Configuration Controller". Therefore, the Applicant's argument is moot in view of the prior art. Further regarding Claim 1, the Applicant alleges that "any programmable indicator in Luan is provided to determine to which bus the memory configuration controller is coupled, and has nothing to do with how that

memory configuration controller issues a request to its respective memory". The Applicant also states that Luan does not teach a system wherein copies of any requested data may be retrieved from either a first or additional storage device". However, Luan discloses the following: "System controller 201 preferably also includes a cache controller 411 for controlling any RAM cache 412 with associated tag RAM 413 optionally included in the system. System controller 201 also includes an arbitration unit 403. Arbitration unit 403 is coupled to shared DRAM controller 409 and to each peripheral controller 106. Arbitration unit 403 receives a memory request signal generated by each peripheral controller 106 when memory access is needed. Arbitration unit 403 determines which requesting bus master is granted access to the shared memory. After selecting a bus master for access grant, arbitration unit 403 sends a "GRANT" signal back to the corresponding peripheral controller 106. Thus during operation, for example a first memory 104 may be configured to operate as dedicated host processor memory while the remaining memories 104 are configured to operate as shared memory. With this configuration, the CPU 101 accesses the first memory 104 without requiring arbitration, as no memory collision can occur with dedicated host processor memory. Simultaneous to CPU 101 accessing first memory 104, peripherals can access any of the shared memory 104. Thus, while CPU 101 is performing peripheral independent operations, and thus is accessing only dedicated host memory, peripherals having bus master capability can independently access shared memory" (Column 9, lines 31-56). Therefore, the Applicant's argument is moot in view of the prior art.

13. With regards to Claim 3, the Applicant alleges that "the cited passage has nothing to do with the memory configuration controller 202 issuing first and second references to two different memories". By reviewing the Examiner's arguments for Claim 1 above, it is clear that Luan

teaches the limitations of Claim 3. Therefore, the Applicant's argument is moot in view of the prior art.

14. Further in regards to Claim 1, the Applicant also states that "there are not multiple copies of any requested data". The Examiner respectfully directs the Applicant to the new 103(a) rejections above. Therefore, the Applicant's argument is moot in view of the prior art.

15. Further in regards to Claim 3, the Applicant alleges that "Luan does not teach the aspect of Claim 3 related to making a determination as to whether a first initiated reference may be fulfilled". However, Luan explicitly states that "Responsive to the received mode select signal being in either a first or second digital state, memory configuration controller 202 couples the memory I/O port to either the SMB 206 or to the HPB 203 respectively" (Column 4,lines 58-60). Therefore, the Applicant's argument is moot in view of the prior art.

16. With regards to Claim 4, the Applicant alleges that "it is not understood how Table 2 in any way teaches that the Luan controller 202 is coupled to two different memory devices". Although Table 2 may not teach the limitations of the claim, the arguments presented by the Examiner in reference to Claim 1 do in fact teach the limitations of Claim 4. Therefore, the Applicant's argument is moot in view of the prior art.

17. Claim 6 stands rejected due to its dependence on Claim 1.

18. With regards to Claim 7, the Applicant alleges that "there is no information regarding how many requests that were issued to the memory required a second reference to complete". However, Luan states that there are "configuration requests, each corresponding to an amount of available system memory" (Column 11, lines 1-3). Therefore, the Applicant's argument is moot in view of the prior art.

19. Further regarding Claim 7, the Applicant alleges that "there can be no mode switch logic in Luan that changes the state of the indicators based on how many requests require a second reference to complete". The Applicant also states that "the Luan system only initiates a single reference to retrieve data when a request is received". However, Luan states "In another aspect of the invention, the programmable shared memory system and method dynamically configures the memory during system start-up in response to a received memory configuration request. Thus, responsive to the memory configuration request, a selected amount of system memory is configured as dedicated processor memory and a selected amount of memory is configured as shared memory (accessible by both the host processor and any system peripherals). Under this programmable architecture, the host processor is provided a dedicated memory space in addition to a memory space shared with system peripherals (a shared memory space)" (Column 2, lines 33-45). Therefore, the Applicant's arguments are moot in view of the prior art.

20. Claims 8 and 10 remain rejected due to their being dependents of Claim 7.

21. With regards to Claim 9, the Applicant alleges that "there is no mode switch logic that switches modes based on the way requests were fulfilled in the past". As stated before however, Luan discloses that this is "programmable architecture" (Column 2, line 42). Therefore, the Applicant's arguments are moot in view of the prior art.

22. With regards to Claim 12, the Applicant alleges that "the cited aspect of Baror has nothing to do with Claim 12, both as currently and as previously presented". Regardless of that fact, Baror does state the following, which teaches the final newly amended portion of Claim 12: "*CBREQ, Cache Burst Request, is an ICU input, synchronous, and active LOW. This input is used to establish a burst-mode cache access on the processor bus and to request the next transfer

during a burst-mode cache access. This signal can become valid late in the cycle compared to *DREQ or *IREQ, to be described hereinafter" (Column 8, lines 5-10). Therefore, the Applicant's arguments are moot in view of the prior art.

23. Further regarding Claim 12, the Applicant alleges that "the MAL...does not appear to be any sort of logic that would store data, or from which requested data may be retrieved". However, Baror states the following: "The memory bus cache instructions are issued by special logic on the memory bus. They allow flexible control of the cache. Cached data can be invalidated, read, and written. The block status can be read and written. A detailed description of the memory bus cache instructions has been set forth hereinbefore" (Column41, lines 36-42). Therefore, the Applicant's arguments are moot in view of the prior art.

24. Claim 13 remains rejected due to it being a dependent of Claim 12.

25. Regarding Claim 14, the Applicant alleges that the operations have "nothing whatsoever to do with data retrieval from two different storage devices". Furthermore, the Applicant states that the reference "does not relate in any way to determining whether any particular storage device must be referenced to complete the data retrieval request". However, Baror states "In the Dragon scheme, all the five block statuses are used. A cache that contains the exclusive modified or shared modified block is its owner. In the case of a miss on read, the block is assigned as shared unmodified or exclusive unmodified depending on the *HIT input. In the case of write hit to a shared block a write-broadcast operation is performed (the memory is not updated) and the block is assigned as shared unmodified or exclusive unmodified according to the *HIT input. Other caches update their own copy of the data. Data intervention is performed by the owner in the case of read match. For this scheme, processor accesses shared bit

assignment is irrelevant, since the *HIT signal is used for this purpose" (Column 44, lines 65-67 and Column 45, lines 1-10). Furthermore, Baror states "In one embodiment, a computer system having a cache memory subsystem in accordance with the invention allows flexible setting of caching policies on a page basis and a line basis. A cache block status field is provided for each cache block to indicate the cache block's state, such as shared or exclusive. The cache block status field controls whether the cache control unit operates in a write-through write mode or in a copy-back write mode when a write hit access to the block occurs. The cache block status field may be updated by either a TLB write policy field contained within a translation look-aside buffer entry which corresponds to the page of the access, or by a second input independent of the TLB entry which may be provided from the system on a line basis" (Column 2, lines 39-51). Therefore, the Applicant's arguments are moot in view of the prior art.

26. Regarding Claim 15, the Applicant alleges that "Baror does not teach initiating a reference to this MAL, which is logic to generate addresses. This logic does not store data, and therefore a data retrieval operation would not be initiated to the MAL. Moreover, Báror does not teach any circuit for determining whether the at least one other memory must be referenced to complete the data retrieval request, and for then initiating data retrieval references based on an identified mode and on that determination". However, the cited material that teaches the limitations of Claim 12 also teach the above limitations of Claim 15. Also, Baror states "a cache block status array configured to store a plurality of cache block status fields, each block status field corresponding to an individual cache block and capable of being set to a write-through state associated with said write-through write mode and to a copy-back state associated with said copy-back write mode; and a control circuit configured to perform a write-through operation in

response to a write hit to a particular cache block associated with a cache block status field which indicates said write-through state and configured to operate in a copy-back mode in response to said write hit if said cache block status field indicates said copy-back state, wherein said control circuit is configured to control said particular cache block status field in response to storing data to said particular cache block in said cache memory subsystem, and wherein said control circuit is further configured to be responsive to said TLB write policy field and to be responsive to said first input line whereby said particular cache block status field can be set to said write-through state if said TLB write policy field indicates said first TLB write policy state and whereby said particular cache block status field can be set to said write-through state if said first input line conveys said write-through status, and wherein said control circuit is configured to set said particular cache block status field to indicate said write-through write mode if said first input line conveys said write-through status, even if said TLB write policy field is set in said second TLB write policy state" (Column 54, lines 11-41). Therefore, the Applicant's arguments are moot in view of the prior art.

27. Regarding Claim 16, the Applicant alleges that "it is not understood how this passage relates in any way to Claim 16". The applicant contests that the material found in the arguments for Claims 12 and 15 adequately teaches the limitations of Claim 16. Therefore, the Applicant's arguments are moot in view of the prior art.

28. Regarding Claim 17, the Applicant alleges that "the MAL does not store data. Moreover, nothing in Barorever contemplates the scenario where the MAL would be unavailable". However, Baror states "As previously indicated, by comparison with the preload instruction, a prefetch operation is defined as the fetching of a variable or an instruction before it is required.

The ICU includes the hardware to support several programmable prefetch options. It also includes a memory read buffer which is used as a prefetch buffer. Prefetched words can be saved in the prefetch buffer if the cache array is not available for the update" (Column 34, lines 37-45). Therefore, the Applicant's arguments are moot in view of the prior art.

29. Further regarding Claim 17, the Applicant alleges that "the Examiner's reasoning set forth in regards to Claim 12, from which Claim 17 depends", does not follow correctly. However, in light of the arguments presented above for Claim 17, the Applicant's arguments are moot in view of the prior art.

30. Regarding Claim 18, the Applicant alleges that "the MAL does most certainly does not include a shared cache". This may very well be true, but Baror states that "A computer system having a cache memory subsystem which allows flexible setting of caching policies on a page basis and a line basis. A cache block status field is provided for each cache block to indicate the cache block's state, such as shared or exclusive. The cache block status field controls whether the cache control unit operates in a write-through write mode or in a copy-back write mode when a write hit access to the block occurs. The cache block status field may be updated by either a TLB write policy field contained within a translation look-aside buffer entry which corresponds to the page of the access, or by a second input independent of the TLB entry which may be provided from the system on a line basis" (Abstract, lines 1-13). Therefore, the Applicant's arguments are moot in view of the prior art.

31. Regarding Claim 19, the Applicant alleges that "the cited Baror passage has nothing to do with the main memory issuing a request to some other memory (e.g. a cache) to retrieve data for that other memory". However, Baror references the "Update memory--An operation that causes

the update of the main memory from the cache. A modified block is written by the cache to the main memory so that the memory is updated with the most current version of the data" (Column 6, lines 1-4). Therefore, the Applicant's arguments are moot in view of the prior art.

32. Claims 20 stands rejected due to its dependence on Claim 12.

33. Regarding Claim 22, the Applicant references the same objections to the Examiner's rejections regarding Claim 12. Therefore, the Examiner respectfully references the rejections cited for Claim 12 as applicable to Claim 22. Therefore, the Applicant's arguments are moot in view of the prior art.

34. Claims 23-29 remain rejected due to their dependence on Claim 22.

35. Regarding Claim 30, the Applicant alleges that "Claim 30 describes first and second cache means that receives requests from the main memory to initiate retrieval of the data". However, Baror references the "Update memory--An operation that causes the update of the main memory from the cache. A modified block is written by the cache to the main memory so that the memory is updated with the most current version of the data" (Column 6, lines 1-4). Therefore, the Applicant's arguments are moot in view of the prior art.

36. Regarding Claim 31, the Applicant alleges that "nothing in Baror teaches the claimed aspect of the invention". However, Baror states "A burst mode memory read access is treated by the ICU as a series of sequential memory read accesses. In the first cycle of a burst mode read access, the address for the first word is transferred by the processor. When a burst mode read access is detected by the ICU, it latches the address and asserts the *CBACK signal" (Column 30, lines 6-11). Therefore, the Applicant's arguments are moot in view of the prior art.

37. Claim 32 remains rejected due to its dependence on Claim 30.

38. Regarding Claim 2, the Applicant alleges that the aspects involved in specifying the sequence in which reference are controlled change "the purpose or functionality of the claimed invention". However, even the Applicant states that the "Specification describes that operation efficiency may be improved" and "without this functionality, the system will not likely run at maximum efficiency, as is the case with prior art systems". Therefore, the Applicant's own words state that the only benefit in providing a specified sequence is to maximize efficiency, which is an obvious improvement for one skilled in the art. Furthermore, the Applicant argues that "the Luan system does not issue first and second references to two different memories to retrieve the same data". However, the Examiner's arguments presented in regards to Claim 1 teach these aspects of Claim 2. Therefore, the Applicant's arguments are moot in view of the prior art.

39. Claim 5 is rejected based on similar arguments for Claim 2.

40. Regarding Claim 11, the Applicant alleges that "nothing in Baror appears to discuss a cache receiving a request from main memory for the return of data". However, Baror states "Data intervention--An operation that can be performed by a slave cache when a match is found in the case of memory-bus read access. If the slave cache contains modified data (the most current version of the data), it intervenes in the access and supplies the data. In this case the main memory should not supply the data" (Column 6, lines 45-50). Baror also states "*DREQ, Data Request, is a synchronous ICU input, active LOW. This input requests a data access on the processor bus. When it is active, the address for the access appears on the Address Bus. For instruction cache usage of the ICU, *DREQ is used for processor-bus cache instruction transfers" (Column 8, lines 62-67). Finally, Baror states that the "MREQT0-MREQT1, Memory Request

Type, is bidirectional, synchronous and three state. These signals specify the address space for the access on the memory bus. When the ICU is the bus master, it uses these signals as outputs. When it is not the bus master, the MREQT signals are used as inputs for data consistency operations" (Column 12, lines 30-37). Therefore, the Applicant's arguments are moot in view of the prior art.

41. Regarding Claim 21, the Applicant alleges that the "register has nothing to do with switching the mode that controls how two different storage devices are accessed". However, Baror states "This logic may be designed according to the specific system organization. It should be capable of monitoring all main memory accesses (this function can be placed in the memory controller)" (Column 45, lines 40-43). Therefore, the Applicant's arguments are moot in view of the prior art.

42. Further regarding Claim 21, the Applicant argues that "many inventions have as their sole purpose the function of performing something automatically that was previously done manually". The Examiner maintains the 103 a rejection, which references Venner, 262 F.2d 91, 95, 120 USPQ 193, 194 (CCPA 1958), where the court held that broadly providing an automatic or mechanical means to replace a manual activity which accomplished the same result is not sufficient to distinguish over the prior art. Therefore, the Applicant's arguments are moot in view of the prior art.

Conclusion

43. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

44. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

45. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lev I. Iwashko whose telephone number is (571)272-1658. The examiner can normally be reached on 9 Hours Schedule), from 8-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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